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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,689	10/28/2003	Pierre Fazan	211.001-D1-US	3924

7590 01/19/2005

Neil Steinberg
Steinberg & Whitt, LLP
Suite 1150
2665 Marine Way
Mountain View, CA 94043

EXAMINER	
LOUIE, WAI SING	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,689	FAZAN ET AL.	
	Examiner	Art Unit	
	Wai-Sing Louie	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because the following deficiencies:

- Fig. 5a, the reference numbers do not agree with the description in the specification.
- Fig. 6a, the reference numbers do not agree with the description in the specification.
- Fig. 7cand 7d, the reference numbers do not agree with the description in the specification.
- Fig. 18, typo error, "shematic" should be "schematic".

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 28-49, 51-54, and 57-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28-63 of copending Application No. 10/724,377. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

With regard to claim 28, Application No. 10/724,377 discloses a semiconductor memory cell including at least one transistor to constitute the memory cell, the memory cell comprising:

- a source region (claim 1);
- a drain region (claim 1);
- a body region disposed between and adjacent to the source region and the drain region, where the body region is electrically floating (claim 1);
- a gate disposed over the body region (claim 1), where the memory cell includes:
    - a first data state representatives of a first charge in the body region (claim 1),
    - a second data state representatives of a second charge in the body region, where the second charge is substantially provided by removing charge from the body region through the source region (claim 1).

With regard to claim 29, Application No. 10/724,377 discloses the first charge is comprised of an accumulation of majority carriers in the body region (claim 30).

With regard to claims 30, 38 and 41, Application No. 10/724,377 discloses the body region is comprised of a p-type semiconductor material and the source and drain regions are comprised of an n-type semiconductor material (claim 50).

With regard to claims 31 and 57, Application No. 10/724,377 discloses the majority carriers accumulate in a portion of the body region that is adjacent to the source region (claim 31).

With regard to claims 32-33, Application No. 10/724,377 discloses positive voltages are applied to the drain region and the gate to remove at least the first charge from the body region (claim 33).

With regard to claims 34-35 and 59, Application No. 10/724,377 discloses in response to the positive voltages being applied to the drain region and the gate, the transistor of the memory cell includes a junction between the body region and the source region, where the junction is forwarded biased (claim 33).

With regard to claims 36, 42 and 44, Application No. 10/724,377 discloses the second charge is stored in the body region in response to removing the positive voltages from the drain region and the gate (claim 36).

With regard to claims 37 and 58, Application No. 10/724,377 discloses a semiconductor memory cell including at least one transistor to constitute the memory cell, the memory cell comprising:

- a source region having impurities to provide a first conductivity type (claim 36);

- a drain region having impurities to provide a first conductivity type (claim 36);
- a body region disposed between and adjacent to the source region and the drain region, where the body region is electrically floating and includes impurities to provide a second conductivity type where the second conductivity type is different from the first conductivity type (claim 36);
- a gate disposed over the body region (claim 1), where the memory cell includes:
    - a first data state representatives of a first charge in the body region where the first charge is substantially provided by impact ionization (claim 36),
    - a second data state representatives of a second charge in the body region, where the second charge is substantially provided by removing charge from the body region through the source region (claim 36).

With regard to claims 39, 48-49, 54, and 60, Application No. 10/724,377 discloses in response to the first positive voltage applied to the drain region and a second positive voltage applied to the gate, at least the first charge is removed from the body region through the source region (claim 36).

With regard to claims 40, 43, 51-53, Application No. 10/724,377 discloses in response to the first and second positive voltages, includes a junction between the body region and the source region, which is forwarded, biased (claim 43).

With regard to claim 45, Application No. 10/724,377 discloses the first charge is stored in the body region in response to applying a first negative voltage to the drain region and a second negative voltage to the gate (claim 38).

With regard to claim 46, Application No. 10/724,377 discloses the transistor of the memory cell stores the first charge in a portion of the body region that is adjacent to the source region (claim 39).

With regard to claim 47, in addition to the limitations disclosed in claim 37, Application No. 10/724,377 also discloses:

- a gate spaced apart from and capacitively coupled to the body region (claim 50).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 50 and 55-56 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 28-63 of copending Application No. 10/724,377 in view of Hamano et al. (US 4,298,962).

With regard to claim 50 and 55-56, Application No. 10/724,377 do not disclose applying ground to the drain region before removing the second voltage from the gate and a third voltage being applied to the drain region before a fourth voltage is applied to the gate. However, Hamano et al. disclose the drain 104 is grounded (col. 6, lines 61-32), and the third (write digit line D_1) voltage is applied to the drain region 104 and the fourth (word line W_2) apply to the gate (col. 6, lines 11-19 and fig. 4). Hamano et al. teach, under such condition, positive voltage could be injected from the source to the channel region and for writing the "0". Application No. 10/724,377 and Hamano et al. have substantially the same environment of memory array having

the transistor memory cell arranged in matrix form. Therefore, it would have been obvious for the one with ordinary skill in the art to modify the device of Application No. 10/724,377 with the teaching of Hamano et al. to apply ground to the drain region and apply a third voltage being applied to the drain region before a fourth voltage is applied to the gate in order to inject positive voltage from the source to the channel for writing the "0".

This is a provisional obviousness-type double patenting rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wsl
January 13, 2005.